REMARKS

Claims 1-4, 6-24, 26-42, 44-51, and 53-70 are pending in the present application and claims 1, 6, 11, 15, 16, 21, 26, 34, 35, 39, 44, 48, 53, 57, and 64 have been amended to further clarify the invention.

Office Action of November 12, 2008

Applicant has carefully reviewed and considered the Office Action of November 12, 2008. Applicant hereby requests entry of this Response and further consideration of the present application in view of the following remarks.

In the Office Action, claims 1-4, 6-20, 39-42, 44-51, and 53-70 were rejected under 35 U.S.C. §102(e) as being anticipated by Srinivasamurthy et al. (U.S. Pat. Pub. No. 2005/0028132 A1), and claims 21-24 and 26-38 were rejected under 35 U.S.C. §102(b) as being anticipated by Warnes (U.S. Pat. No. 7,051,189). Applicant respectfully traverses these grounds of rejection and requests reconsideration thereof.

Support For Claim 21

The Examiner requested that Applicant to point out the support for the amended claim 21, specifically, the support for "modifying the frequency of the use of the register by performing a loop analysis."

Claim 21 has been amended and the passage in question has been amended to further clarify the invention. The amended is fully supported by the specification as follows. The present invention is directed toward methods for optimizing a code sequence (Abstract) and the optimization may be done by analyzing the frequency of use of registers (FIG. 4, [0060]). The optimization may be done by a compiler performing a loop analysis to modify the histogram to take into account instructions that occur within loops that may get executed multiple times ([0059]). The histogram represents the frequency of operation and is developed by the compiler ([0048]).

Applicant submits that amended claim 21 is fully supported as shown above.

Rejection Under 35 U.S.C. §102(e)

Claim 1

The Office Action rejected claim 1 under 35 U.S.C. §102(e) and stated that Srinivasamurthy et al. discloses every elements of claim 1. Applicant respectfully disagrees with the Examiner's interpretation. Specifically, the Office Action stated that Srinivasamurthy et al. discloses performing a loop analysis to determine a static frequency of operations in the code sequence and cited paragraphs [0045]-[0046] and [0049]-[0050] of Srinivasamurthy et al. as support. Upon a close review of the cited paragraphs, Applicant submits that "loop" is used in Srinivasamurthy et al. as "interpreter loop" and also as "JVM interpreter loop." It seems that "interpreter loop" in Srinivasamurthy et al. refers to an interpretation function and not a code sequence that is executed multiple times. Because in paragraph [0067] of Srinivasamurthy et al. it is stated that "the JVM interpreter loop is modified to detect and execute the new sEc opcode 31." It can be concluded from this paragraph that the interpretation function can be modified to detect and execute new sEc opcode and not modifying a "loop" of a code sequence.

Notwithstanding the above, Applicant has amended claim 1 to further distinguish from the cited reference and clarify the loop analysis. Applicant submits that amendment is fully supported by the specification ([0059]) and no new matter is introduced.

Applicant submits that Srinivasamurthy et al. does not disclose at least the element of determining an executed frequency of operations within multiple times executed loops for the code sequence of amended claim 1 and as result Srinivasamurthy et al. cannot anticipate amended claim 1. Therefore, Applicant respectfully requests the rejection be withdrawn and amended claim 1 be allowed.

Claims 2-4 and 7-10

Claims 2-4 and 7-10 depend from amended claim 1 and Applicant submits that they are allowable for at least the reasons stated above with respect to the patentability of amended claim 1.

Claim 6

The Office Action failed to state the reason for which claim 6 is rejected. 37 CFR 1.104 states that when a reference is complex, the part relied by the examiner to reject a claim "must be designated as nearly as practicable." Nevertheless, Applicant has amended claim 6 to further clarify the claimed invention. The amendment is fully supported by the specification ([0067]) and no matter is introduced. Applicant respectfully requests the Examiner to distinctly point out where in the cited reference it is disclosed op-code being executed by a loadable microcode.

Claim 11

The Office Action stated that Srinivasamurthy et al. discloses "providing a plurality of pre-determined instructions" and cited paragraphs [0021], [0030], [0046], [0049], and [0066]-[0068] as support. Upon a close review of the cited paragraphs, it seems that in [0030] it is stated that FIG. 3 "illustrates two examples of basic block bytecode sequences... used for performance comparison." Again in paragraph [0074], Srinivasamurthy et al. states "the dot-product benchmark was used to study the speedup of the JVM" and "consideration was restricted to the two basic block bytecode sequences as shown in FIG. 3." Applicant submits that Srinivasamurthy et al. does not disclose "providing a plurality of pre-determined instruction sets with each pre-determined instruction set comprising instructions including assigned op-code representations."

However, in an effort to move forward the present application, claim 11 has been amended to further clarify that each pre-determined instruction set provided is optimized for a frequency of a particular operation. Amendment is fully supported by the specification ([0057]) and no new matter is introduced.

Applicant submits that Srinivasamurthy et al. does not disclose at least the element of providing plurality of pre-determined instruction sets as of amended claim 11 and as result Srinivasamurthy et al. cannot anticipate amended claim 11. Therefore, Applicant respectfully requests the rejection be withdrawn and amended claim 11 be allowed.

Claims 12-14 and 17-20

Claims 12-14 and 17-20 depend from amended claim 11 and Applicant submits that they are allowable for at least the reasons stated above with respect to the patentability of amended claim 11.

Claims 15

Claim 15 has been amended to clarify the loop analysis. Applicant submits for the same reasons stated above with regard to the patentability of amended claim 1 that Srinivasamurthy et al. does not disclose determining operation frequency further comprising determining an executed frequency of operations within multiple times executed loops for the code sequence and as result Srinivasamurthy et al. cannot anticipate amended claim 15. Therefore, Applicant respectfully requests the rejection be withdrawn and amended claim 15 be allowed.

Claim 16

The Office Action stated that Srinivasamurthy et al. discloses modification of the op-code may be executed by a loadable microcode. Applicant disagrees with the Examiner's interpretation of paragraphs [0067] and [0069]. The cited paragraphs seem to disclose a class loader that is an external tool capable of replacing Sec-opcode at the runtime and tracking calls. It is stated in [0069] that the sEc-hook helps the class loader to pinpoint the method, location and size of the bytecode stream to be rewritten in the corresponding sEc-opcode.

Claim 16 has been amended to further clarify the invention. The loadable microcode of amended claim 16 is one embodiment of the invention that maybe loaded from an external source. The amendment is fully supported by the specification ([0067]) and no matter is introduced.

Applicant submits that Srinivasamurthy et al. does not disclose at least the loadable microcode of amended claim 16 and as result Srinivasamurthy et al. cannot anticipate amended claim 16. Therefore, Applicant respectfully requests the rejection be withdrawn and amended claim 16 be allowed.

Claim 21

The Office Action stated that Warnes discloses determining a frequency of use of a register and modifying the frequency of use of the register by performing a loop analysis. Applicant respectfully disagrees with the Examiner's interpretation.

Warnes discloses determining a static frequency of each instruction type (col. 9, lines 4-5) and also encoding of registers (col. 11, 15-16) for faster and simpler decoding (col. 12, liens 15-16). However, Warnes does not teach disclose determining a frequency of use of registers or modifying a static frequency of operations by analyzing multiple time executed loops to determine an executed frequency of operations in the register as amended claim 21.

Therefore, Applicant submits that Warnes cannot anticipate amended claim 16 and allowance thereof is respectfully solicited.

Claims 22-24 and 27-29

Claims 22-24 and 27-29 depend from amended claim 21 and Applicant submits that they are allowable for at least the reasons stated above with respect to the patentability of amended claim 21.

Claims 26 and 35

The Office Action stated that Warnes discloses elements of claims 26 and 35 and pointed to 12 columns of text (col. 11, line 21 to col. 22, line 64) in Warnes as the support. 37 CFR 1.104 states that when a reference is complex, the part relied by the examiner to reject a claim "must be designated as nearly as practicable." Upon a cursory review of 12 columns, Applicant does not discern where loadable microcode is disclosed.

Nevertheless, Applicant has amended claims 26 and 35 to further clarify the claimed invention. The amendment is fully supported by the specification ([0067]) and no matter is introduced. Applicant respectfully requests the Examiner to distinctly point out where in the cited reference it is disclosed op-code being executed by a loadable microcode.

Claim 30

The Office Action stated that Warnes discloses limiting the use of one or more of the plurality of registers. Applicant disagrees with the Examiner's interpretation of the cited reference. Upon a close review, the cited passage (col. 11, Table 3, col. 11:14-col. 12:61), it seems that Warnes discloses encoding of registers (Table 3) for faster and simpler instruction decoding (col. 12, lines 14-15), but not limiting number of registers available for use as claim 30.

Therefore, Applicant submits that Warnes does not disclose limiting use of one of more registers and cannot anticipate claim 30. Applicant respectfully requests rejection be withdrawn and claim 30 allowed.

Claims 31-33 and 36-38

Claims 31-33 and 36-38 depend from claim 30 and Applicant submits that they are allowable for at least the reasons stated above with respect to the patentability of claim 30.

Claims 34

Claim 34 has been amended to clarify the loop analysis. Applicant submits for the same reasons stated above with regard to the patentability of amended claim 1 that Warnes does not disclose determining operation frequency further comprising determining an executed frequency of operations within multiple times executed loops for the code sequence and as result Warnes cannot anticipate amended claim 34. Therefore, Applicant respectfully requests the rejection be withdrawn and amended claim 34 be allowed.

Claim 39

Claim 39 is similar in scope to amended claim 1 and Applicant submits that amended claim 39 is allowable for the same reasons stated above with respect to the patentability of amended claim 1.

Claims 40-42 and 45-47

Claims 40-42 and 45-47 depend from amended claim 39 and Applicant submits that they are allowable for at least the reasons stated above with respect to the patentability of amended claim 39.

Claim 44

Claim 44 is similar in scope to amended claim 16 and Applicant submits that amended claim 44 is allowable for the same reasons stated above with respect to the patentability of amended claim 16.

Claim 48

The Office Action stated that Srinivasamurthy et al. discloses every elements of claim 48, specifically, the Office Action stated that Srinivasamurthy et al. discloses performing a loop analysis to determine a static frequency of operations in the code sequence and cited same paragraphs [0045]-[0046] and [0049]-[0050] cited for rejection of claim 1 as support. Applicant respectfully disagrees with the Examiner's interpretation of cited reference.

However, claim 48 has been amended to further clarify the loop analysis. Applicant repeats the arguments presented in regard to patentability of amended claim 1 and submits that Srinivasamurthy et al. cannot anticipate amended claim 48 for failing to disclose at least the element of determining an executed frequency of operations within multiple times executed loops for the code sequence.

Claims 49-51 and 54-56

Claims 49-51 and 54-56 depend from amended claim 48 and Applicant submits that they are allowable for at least the reasons stated above with respect to the patentability of amended claim 48.

Claim 53

Claim 53 is similar in scope to amended claim 16 and Applicant submits that amended claim 53 is allowable for the same reasons stated above with respect to the patentability of amended claim 16.

Claim 57

Claim 57 has been amended to further distinguish the claimed invention from the cited reference, specifically, claim 57 has been amended to clarify that determination of a static frequency of operations and an executed frequency of operations is done by analyzing loops performed by the source code. As discussed above with regard to the patentability of claim 1, Srinivasamurthy et al. does not disclose a loop analysis as amended claim 57. Therefore, Applicant submits Srinivasamurthy et al. cannot anticipate amended claim 57 and allowance thereof is respectfully solicited.

Claims 58-63

Claims 58-63 depend from amended claim 57 and Applicant submits that they are allowable for at least the reasons stated above with respect to the patentability of amended claim 57.

Claim 64

Claim 64 has been amended to clarify that tuning an instruction set is by selecting an op-code representation from a plurality of pre-determined sets. As discussed with regard to the patentability of claim 11, Srinivasamurthy et al. does not provide a plurality of pre-determined op-codes to be selected when tuning an instruction set. Therefore, Applicant submits Srinivasamurthy et al. cannot anticipate amended claim 64 and an early notification of allowance thereof is respectfully solicited.

Claims 65-70

Claims 65-70 depend from amended claim 64 and Applicant submits that they are allowable for at least the reasons stated above with respect to the patentability of amended claim 64.

Conclusion

In view of the foregoing remarks, Applicant respectfully submits that Claims 1-4, 6-24, 26-42, 44-51, and 53-70 are in condition for allowance and entry of the present amendment and notification to that effect is earnestly requested. If necessary, the Examiner is invited to telephone Applicant's attorney (770-246-2599) to facilitate prosecution of this application.

No additional fees are believed due. However, the Commissioner is hereby authorized to charge any additional fees that may be required, including any necessary extensions of time, which are hereby requested to Deposit Account No. 50-4290.

Respectfully submitted,

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